

# EMSAT Rules Short Descriptions

The following is a short description for each **EMSAT** EMC rule. In most cases, each rule has many more optional parameters that may be set by the user. These short descriptions describe the most important options.

## Signal Reference Rules

### **Critical Net Crossing Split Reference Plane**

*Rule Statement:*

Critical nets must not cross a split in the adjacent reference plane.

*Major Options:*

1. Any crossing of an adjacent plane by a critical net will cause a violation.
2. A cross is allowed if two stitching capacitors (one on either side of the crossing point) are within a specified distance of the crossing.

### **Critical Net Changing Reference Plane**

*Rule Statement:*

Critical nets must not change reference planes.

*Major Options:*

1. Any change in reference plane for a critical net will cause an violation.
2. Reference plane crossing is allowed if two decoupling capacitors (or vias if the planes are the same net name) are within a specified radial distance from the signal via where the signal changes reference planes.
3. Reference plane crossing is allowed if three decoupling capacitors (or vias if the planes are the same net name) are within a specified radial distance from the signal via where the signal changes reference planes.
4. Ignore initial via when within specified distance from IC pin (transmit or receive).

### **Net Near Edge of Reference Plane**

*Rule Statement:*

Critical nets may not be within a specified distance of the edge of their reference plane.

*Major Options:*

1. Specified distance from edge of plane may be different for external and internal signal layers.
2. Distance to edge of board may be checked instead of edge of plane.
3. Edge connector traces may be ignored.

## Wiring and Crosstalk Rules

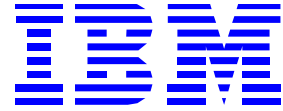
### **Critical Net Near I/O net**

*Rule Statement:*

Critical nets may not be routed within a specified distance form an I/O net.

*Major Options:*

1. Class of I/O net can be specified.



### **Length of Exposed Critical Traces**

*Rule Statement:*

All critical nets must be buried between solid planes. The allowable length of the exposed portion of a critical net may be specified.

*Major Options:*

1. All critical nets, single ended critical nets only, or I/O net only may be selected.

### **Critical Net Isolation (Single-Ended Nets)**

*Rule Statement:*

All critical nets must have a "ground-guard" trace on either side of the critical net.

*Major Options:*

1. Vacant trace isolation may be used in place of ground-guard traces.

### **Critical Net Isolation (Differential Nets)**

*Rule Statement:*

All differential critical nets must have a "ground-guard" trace on either side of the differential pair of nets.

*Major Options:*

1. Vacant trace isolation may be used in place of ground-guard traces.

### **Critical Differential Net Length Matching and Spacing**

*Rule Statement:*

All critical nets must be routed within a specified distance of each other, and the length of the differential pair of nets must match within a specified amount.

### **Wide Power/Ground Traces**

*Rule Statement:*

All power and ground traces longer than a specified distance must be wider than another specified distance. This does not include grounded guard traces.

## **Decoupling Rules**

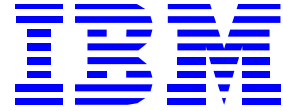
### **Decoupling Capacitor Density**

*Rule Statement:*

Decoupling capacitors must be placed between all adjacent plane pairs within a specified grid density.

*Major Options:*

1. Decoupling power/ground-reference pairs rather than adjacent pairs of planes.
2. Number of decoupling capacitors required within each grid location.
3. Allow via to connect planes of same net name rather than use capacitor.



### **Decoupling Capacitor Distance from IC Power Pin**

*Rule Statement:*

A decoupling capacitor must be connected between the power and ground-reference planes and be placed within a specified distance from each IC power pin.

*Major Options:*

1. Allow capacitors on back side of the board.

### **IC Power/Ground-Reference Pin Distance to Via**

*Rule Statement:*

The trace connecting between the IC power and/or ground reference pin to the associated via to the power/ground-reference plane must be no longer than the specified distance.

*Major Options:*

1. Distance to search beyond specified distance for via.

### **Decoupling Capacitor Distance to Via**

*Rule Statement:*

The trace connecting between a decoupling capacitor to the associated via to the power/ground-reference plane must be no longer than the specified distance.

*Major Options:*

1. Distance to search beyond specified distance for via.

### **Power/Ground-Reference Trace Decoupling**

*Rule Statement:*

All power and ground-reference traces longer than a specified length must have a decoupling capacitor within a specified distance from the IC power pin.

## **Placement Rules**

### **I/O Filter Net Distance**

*Rule Statement:*

All I/O filters must be placed within a specified distance from the I/O connector.

*Major Options:*

1. Select all I/O nets or combinations of Class 1L, Class 1H, Class 2 and/or Class 3 I/O nets.

### **Distance from Oscillator to Clock Driver**

*Rule Statement:*

All Oscillators must be placed within a specified distance from the clock driver (or other device) that they drive.